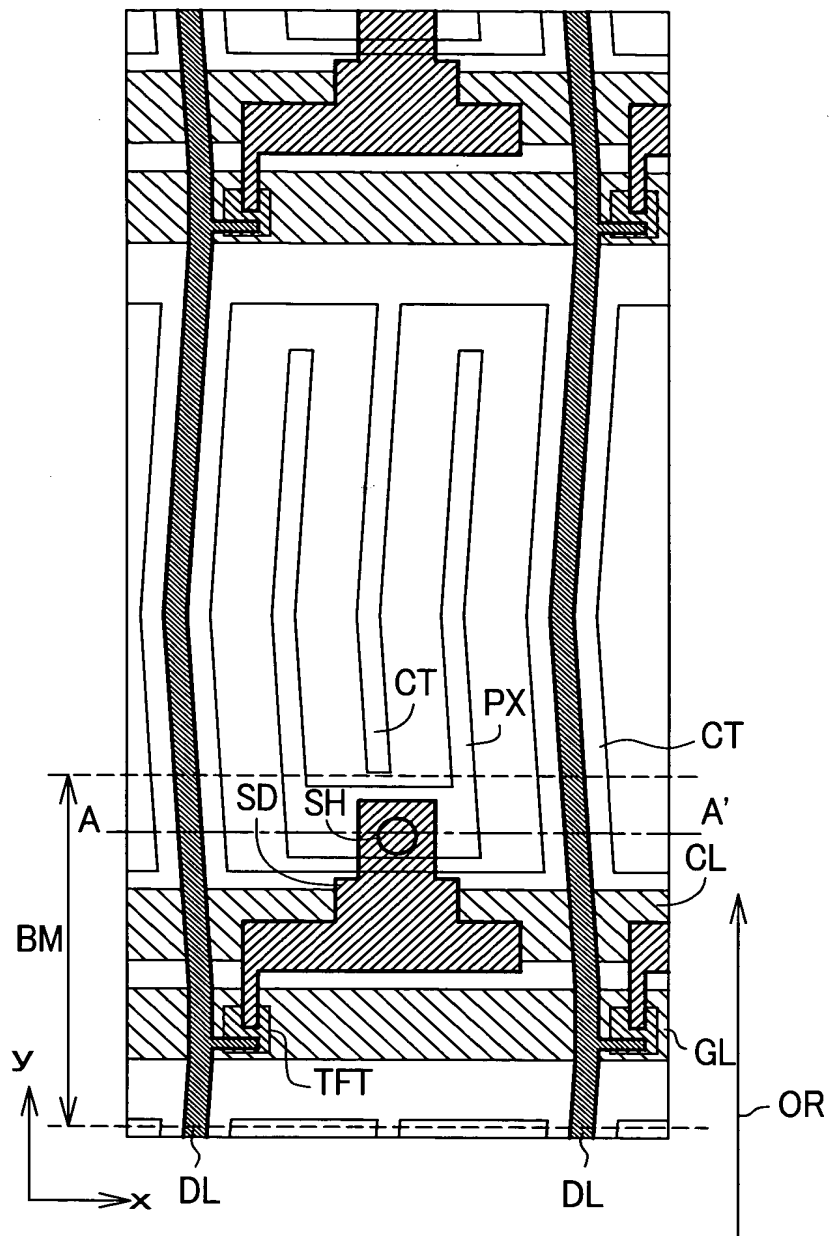
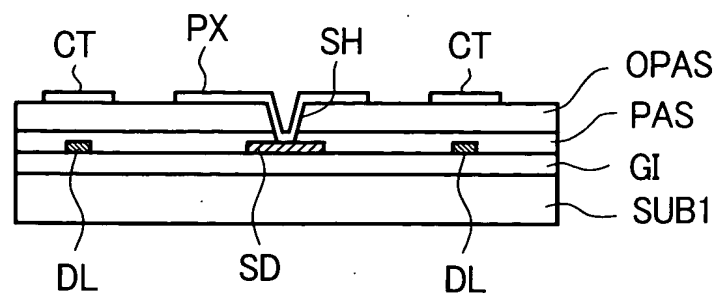


*FIG. 1A*



*FIG. 1B*

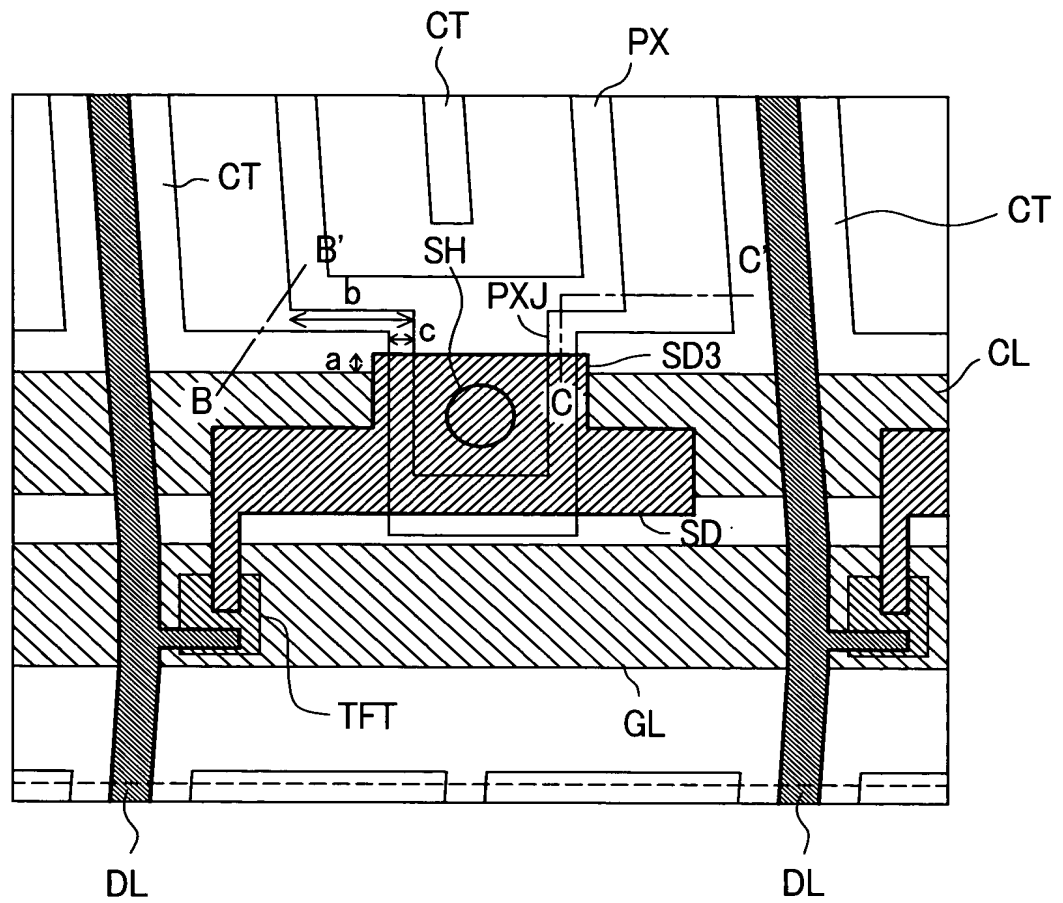


[illegible]

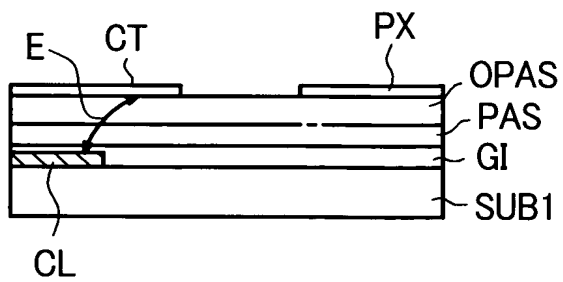
A cross-sectional view of a semiconductor device. The device consists of a substrate layer labeled SUB1. Above SUB1 is a gate insulating layer labeled GI. Above GI is a passivation layer labeled PAS. Above PAS is an organic passivation layer labeled OPAS. A contact layer labeled CL is located on the SUB1 layer. A contact pad labeled CT is located on the CL layer. A pixel labeled PX is located on the OPAS layer.

This diagram shows a cross-sectional view of a liquid crystal cell assembly. The assembly consists of two glass substrates, labeled GL, which are separated by a spacer. The spacer is formed by two vertical bars, labeled DL, and a central block, labeled PX. The central block PX is surrounded by a layer of liquid crystal material, labeled CT. The liquid crystal material CT is also shown in the central region of the cell. The glass substrates GL are shown with various layers, including a top layer labeled BM and a bottom layer labeled TFT. A central region of the glass substrates is labeled SD. The assembly is shown in a cross-section along the x-y plane, with a dashed line indicating the center of the cell. The distance between the two glass substrates is labeled A. The distance between the two vertical bars DL is labeled BM. The distance between the two vertical bars DL is also labeled A'. The distance between the two vertical bars DL is also labeled A''. The distance between the two vertical bars DL is also labeled A'''. The distance between the two vertical bars DL is also labeled A''''. The distance between the two vertical bars DL is also labeled A''''.

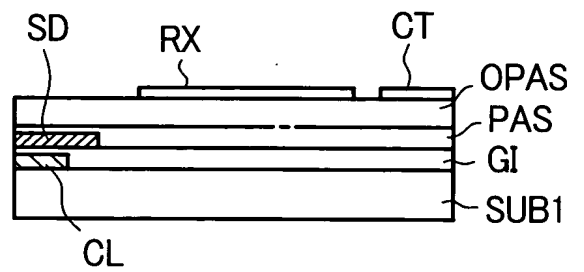
**FIG. 4A**



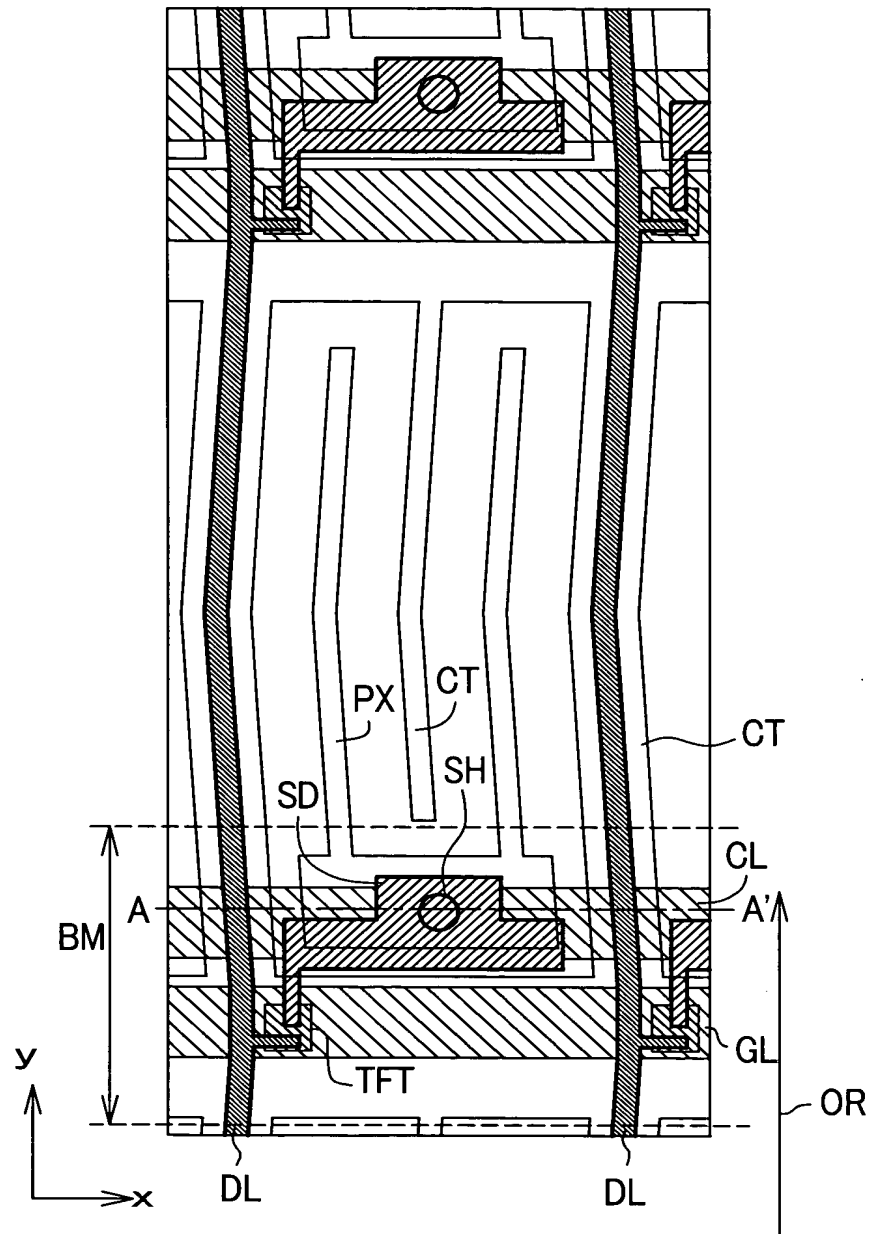
**FIG. 4B**



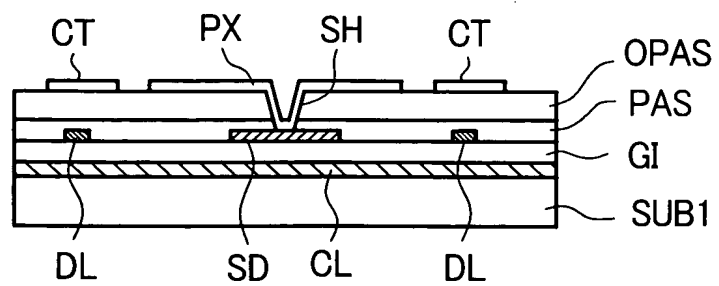
**FIG. 4C**



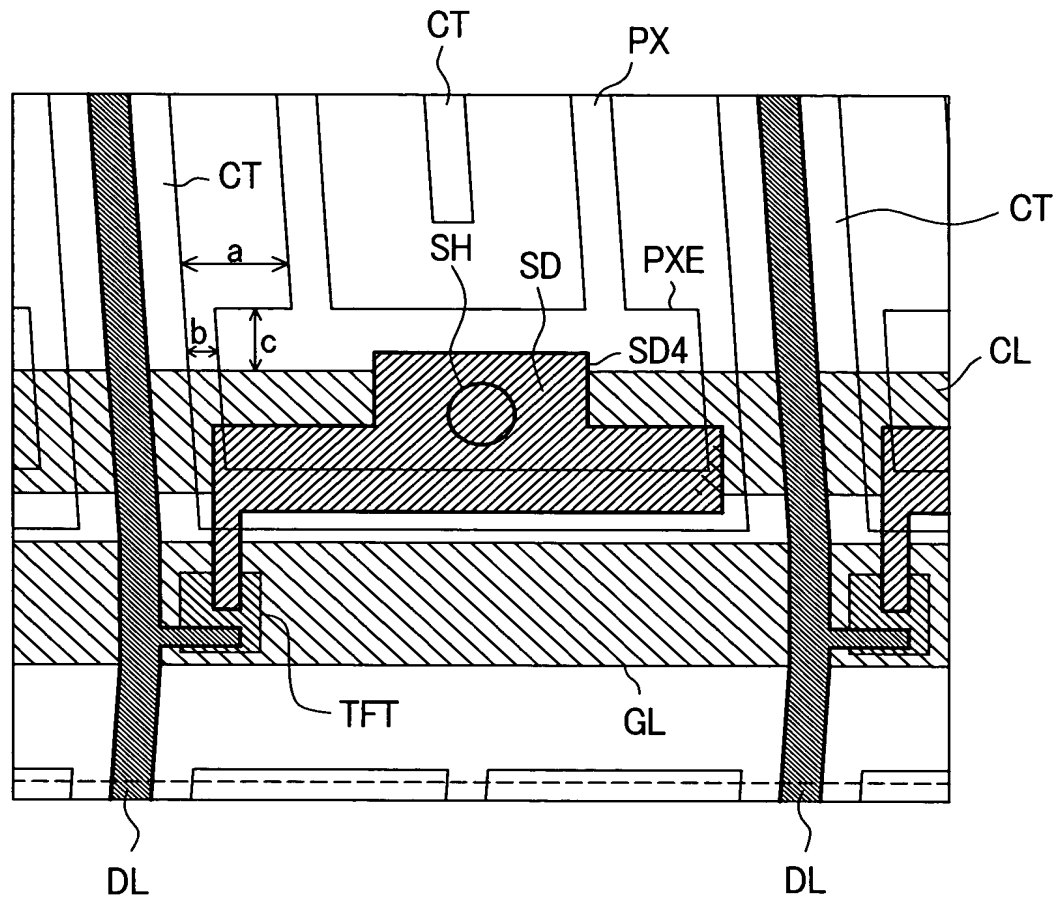
*FIG. 5A*



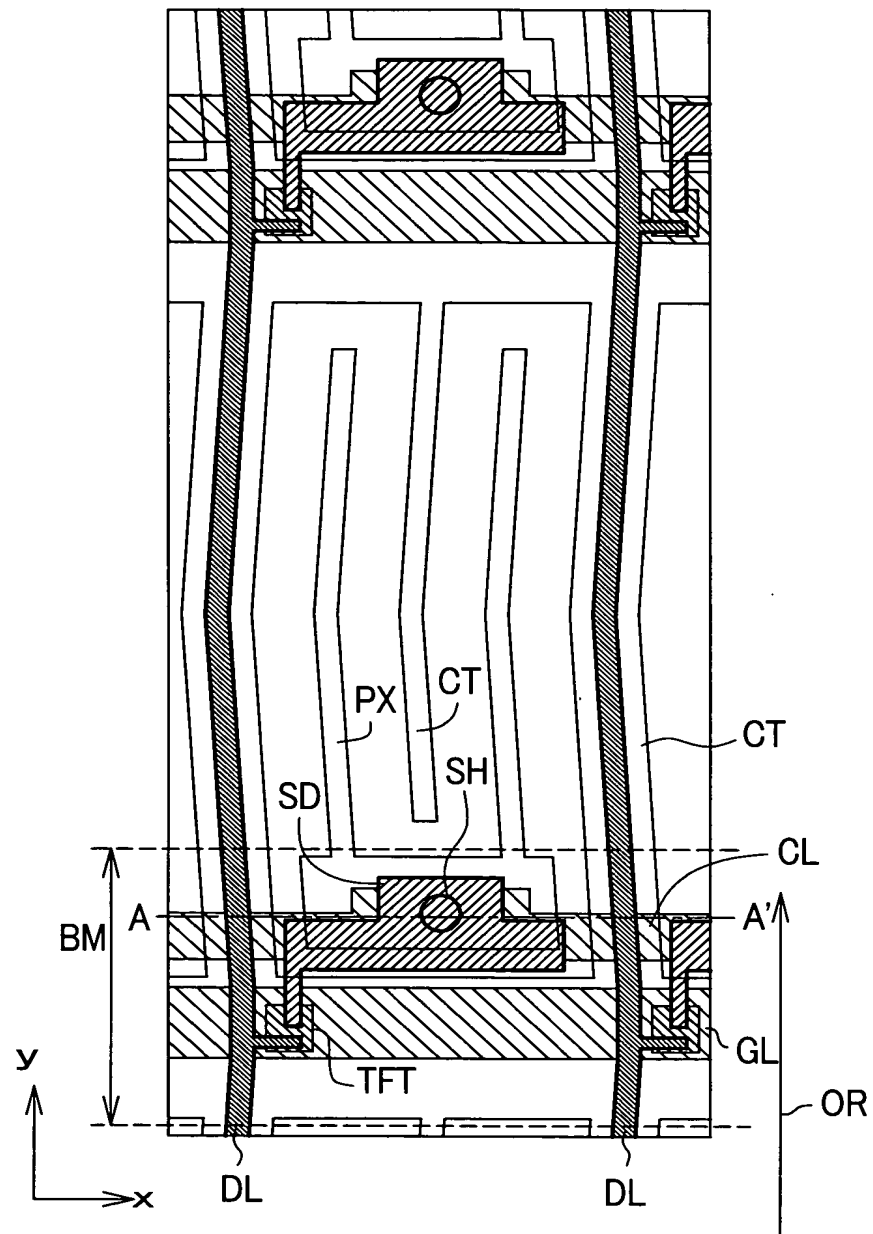
*FIG. 5B*



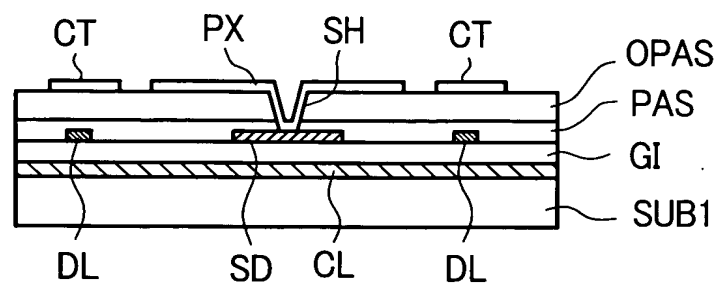
*FIG. 6*



*FIG. 7A*



*FIG. 7B*



*FIG. 8*

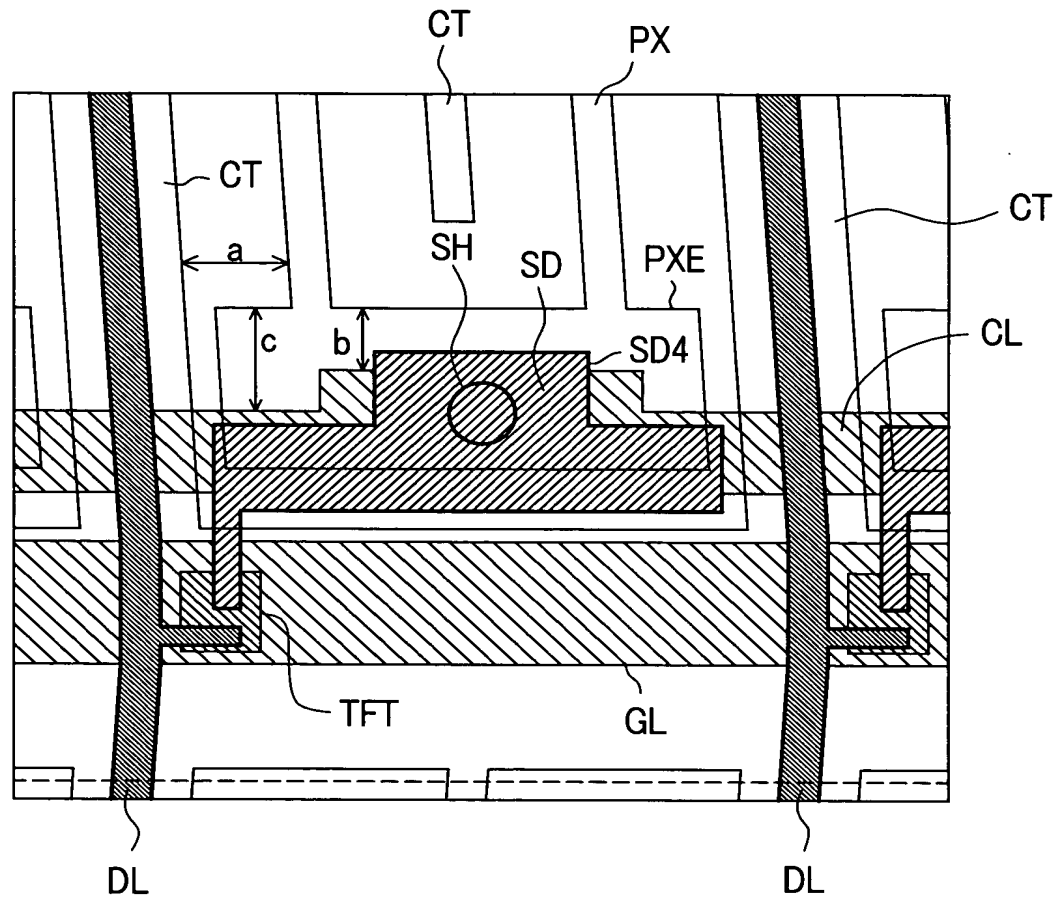
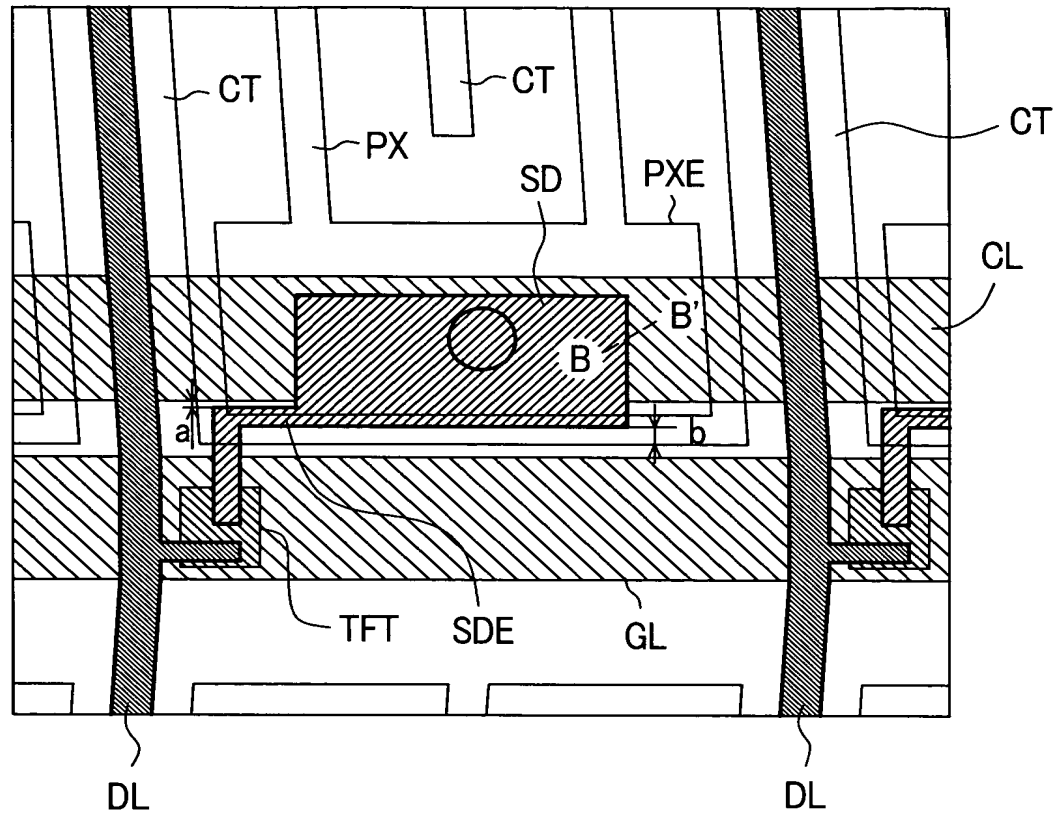


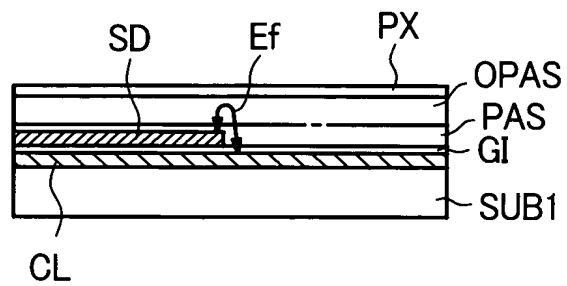


Fig. 1 is a cross-sectional view of a semiconductor device. The device is built on a substrate (SUB1) which contains layers DL, SD, CL, and DL from top to bottom. A gate stack (GI) is formed on top of the substrate. Above the gate stack is a passivation layer (PAS) and an organic passivation layer (OPAS). A central trench is formed in the OPAS layer, filled with a conductive material (SH), and surrounded by a conductive layer (PX). The device is protected by a conductive layer (CT) on the sides.

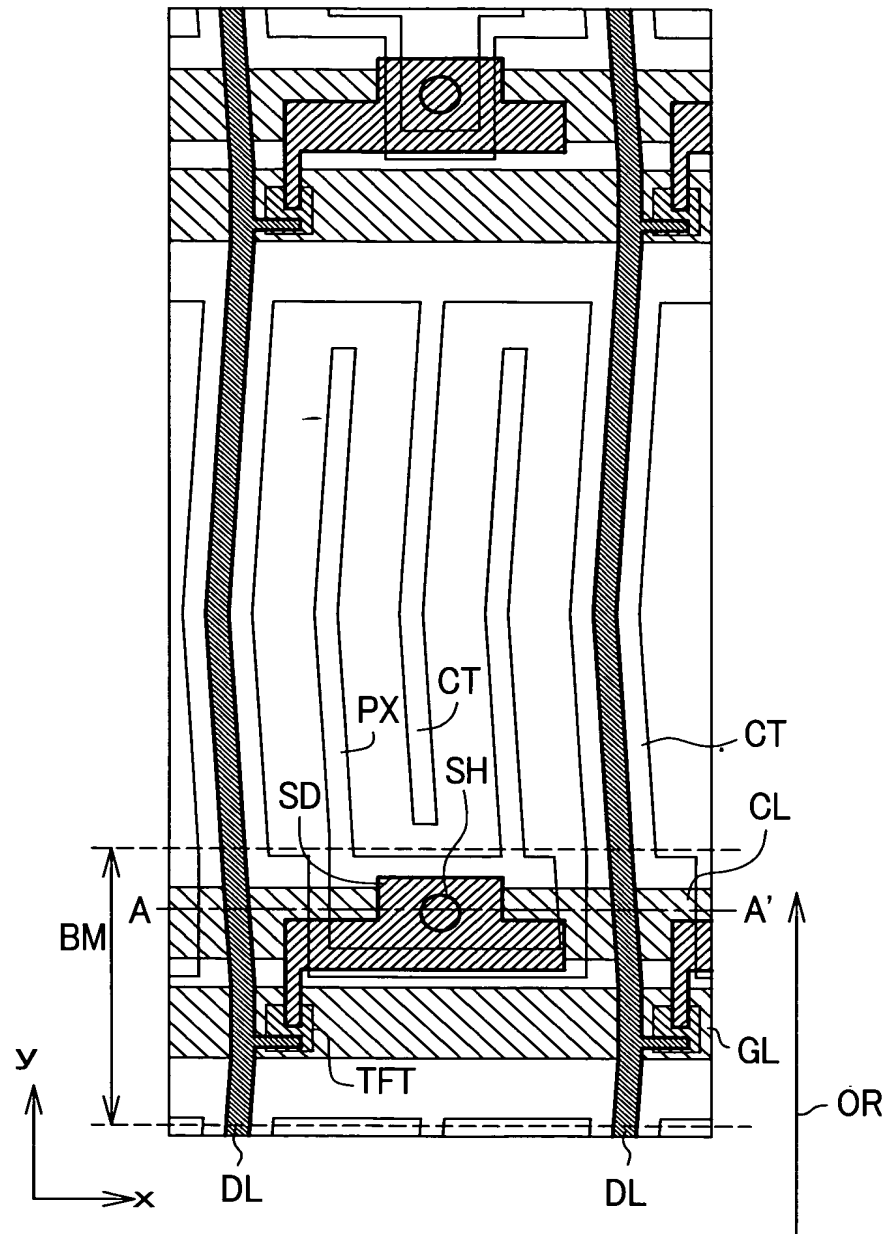
*FIG. 10A*



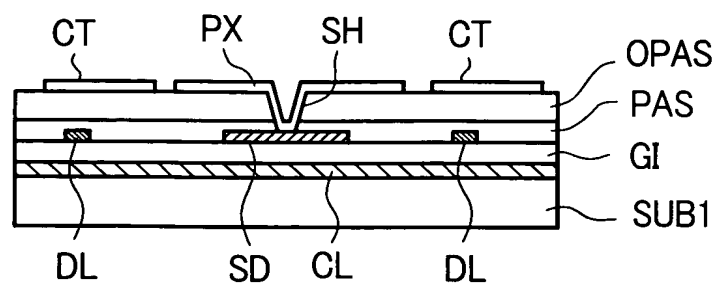
*FIG. 10B*



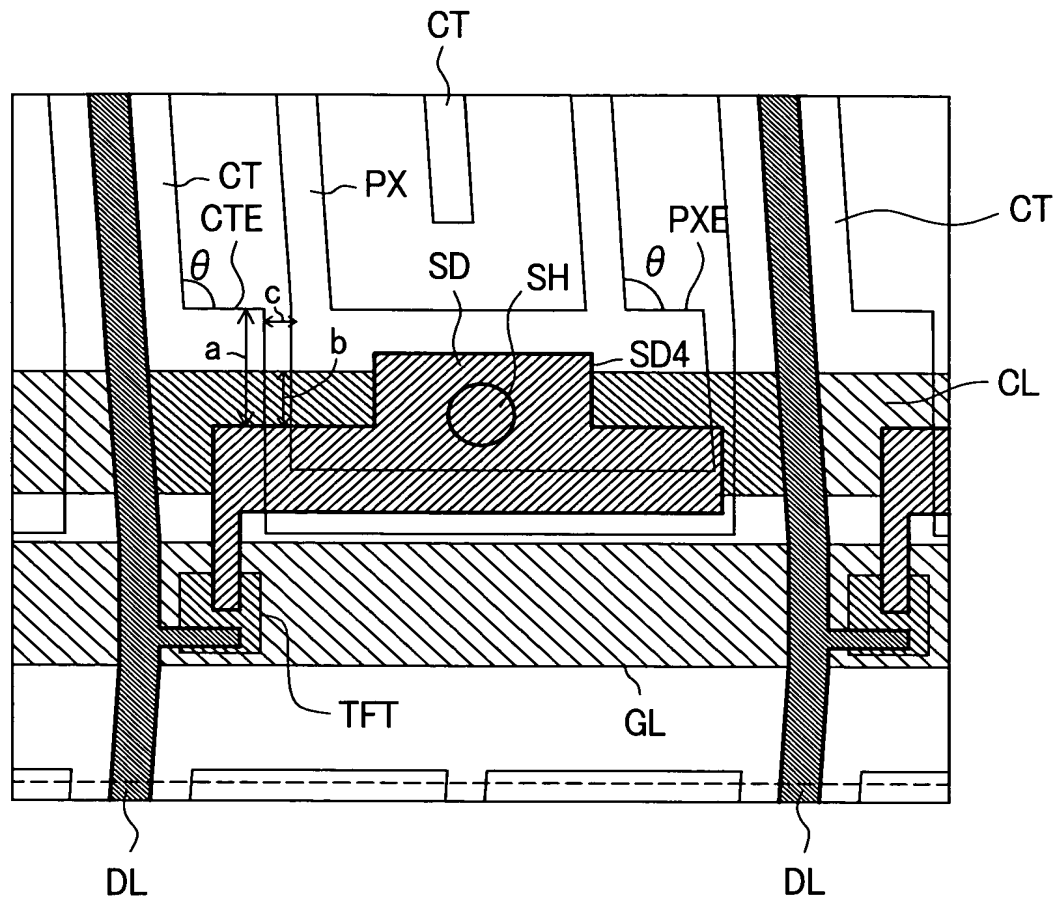
*FIG. 11A*



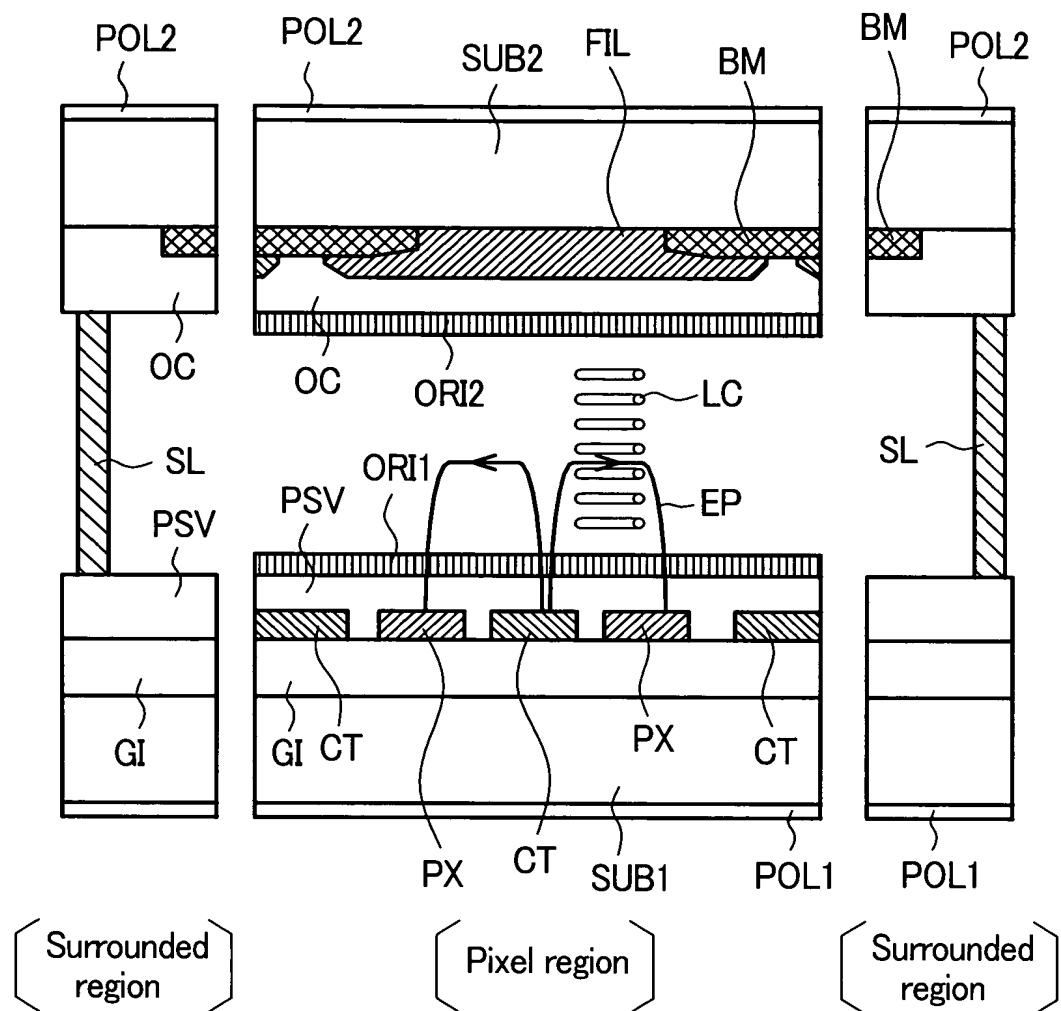
*FIG. 11B*



*FIG. 12*



*FIG. 13*



A detailed cross-sectional diagram of a semiconductor device. The diagram shows a central region with two vertical pillars labeled CT and PX. Between these pillars is a structure labeled SH. To the left of SH is a layer labeled SD. Below the central region is a horizontal layer labeled CL. Below CL is a layer labeled A, which is part of a larger structure labeled BM. Below A is a layer labeled A', which is part of a larger structure labeled GL. Below GL is a layer labeled TFT. At the bottom are two vertical structures labeled DL. The entire device is mounted on a substrate labeled OR. A coordinate system is shown at the bottom left with a vertical y-axis and a horizontal x-axis.

A cross-sectional view of a semiconductor device. The device features a central region with a circular hole, surrounded by a layer labeled SD. Above this, a layer labeled SH is shown. The top surface is labeled PX. The side walls are labeled CT. The bottom surface is labeled GL. The device is flanked by two vertical structures labeled DL. The central region is also labeled B' and B. The bottom surface is also labeled C and C'. The side walls are also labeled CL. The bottom surface is also labeled TFT.

A cross-sectional view of a semiconductor device. It shows a substrate (SUB1) with several layers: a bottom layer (CL), a gate insulator (GI), a passivation layer (PAS), and an organic passivation layer (OPAS). A patterned layer (PX) is formed on top of the OPAS layer. An electrode (E) is formed on the PX layer, and a curved arrow indicates an electric field (E) between the electrode and the CL layer.

Diagram illustrating a cross-sectional view of a semiconductor device. The structure includes a substrate (SUB1) with layers (GI, PAS, OPAS) and a curved electrode (E) with a contact (CT). A source-drain region (SD) is shown with a gate (Ef) and a channel (CL).